REMARKS/ARGUMENTS

Claims 1 - 7, and 9 - 21, and 23 - 24 remain in the application. Claims 8, 22, and 25 – 34 have been cancelled.

Examiner Kennedy is thanked for carefully reviewing the subject patent application. All claims under consideration are now believed to be in allowable condition, and allowance is so requested.

I. Rejection under 35 U.S.C. 103 (a)

Reconsideration of the rejection of claims 1 - 24 under 35 USC 103 (a) as being unpatentable over Applicants admitted prior art (AAPA) in view of Huang et al. (U.S. Patent 5,747,382) and Park (U.S. Patent 6,025,223) is requested, in light of the following.

The Applicants respectfully submit that AAPA does not teach a method of "performing a CMP step to planarize said insulation layer". On page 4, lines 6 - 17, the CMP process initially mentioned in lines 1-5 is further described as inadequate because "the thickness loss t_2 typically varies across the wafer" (line 10) and the "distance (t_1-t_2) ..... cannot be adequately controlled" (lines 12-14). Furthermore, the AAPA does not teach a method to minimize the cap layer thickness loss t_2, minimize the variation (t_1-t_2), or minimize the "certain thickness below the cap layer" which is distance "d" in FIG. 4. The applicants state on page 5, lines 1-2, that "a better method is needed to controllably form a more planar insulation layer 5 with less cap layer thickness loss" which implies that a partial planarization by the AAPA CMP process is not acceptable and therefore not recommended.

The Applicants wish to point out that when the distance "d" is large as in prior art, cap layer thickness t_1 must be increased accordingly to prevent electrical shorting from second conductive line 6 (FIG. 1) to bottom portion 4a (FIG. 4). In other words, bit line to free layer distance is increased in the MRAM. As a result, bit line switching current must be increased and this leads to higher power consumption and poor device performance as appreciated by those skilled in the art. In comparison, the Applicants' process allows a thinner cap layer to be employed because of reduced cap layer thickness loss. Furthermore, the variation in dielectric layer thickness x_3 is substantially less than "d" as stated on page 14, lines 12-15.

With regard to the Examiner's statement on page 7 of the Office Communication that "Applicant has provided only an advantage to having the cap layer thickness variation of less than +/- 5 Angstroms", the Applicants wish to point out that this is a significant advantage which allows bit line switching field variation to be controlled within tighter limits and thereby improve device performance. Moreover, the etch uniformity of +/- 5% (col. 3, line 21) in Huang refers to the thickness of the IMD layer and not to a cap layer in the MTJ element as in the claimed invention. The ability to control the cap layer thickness variation coupled with a second advantage which is a tighter control of the protrusion "x_3" of the cap layer to a distance of about 50 to 190 Angstroms (page 14, lines 8 - 10) has not been achieved in prior art. Regarding the Examiner's comments in the second paragraph on page 7 of the office communication, the Applicants respectfully submit that the advantages of the claimed invention are stated on page 13, lines 21 - 23 and continuing on page 14, lines 1 to 3. In particular, the thickness variation after the etch back step is within $\pm$ 5

Angstroms compared to the prior art variation of ± 40 Angstroms. Furthermore, "The etch back planarization step results in a top surface 30 of the second insulation layer 27 that is more uniform than in prior art methods....." as stated on page 14, lines 20 - 22.

With regard to the Examiner's statement on page 3 of the office communication that "Park discloses the method wherein the insulating layer is planarized at a certain distance below said cap layer", the Applicants respectfully submit that Park does not teach planarization of the insulating layer 36 and insulating spacer 36a. The as-deposited dielectric layer 36 is understood not to be planar by those skilled in the art because it is deposited over topography. Moreover, the terms "planar" or "planarized" are not found in the Park specification. Although FIG. 9 shows what appears to be a planar surface on the etched back dielectric layer 36a, those skilled in the art will recognize that only a narrow cross-section of the device is shown. The pattern depicted in FIG. 9 is not uniform across the wafer and there are regions (not shown) having larger gaps between capacitor layers. In the larger gap regions, the thickness of layer 36a is understood to be thinner than in the portion of layer 36a shown in FIG. 9. This reasoning is substantiated in Huang (U.S. 5,747,382) in col. 1, line 58 through col. 2, line 7. In particular, an "SOG layer 16" is formed over a line pattern similar to the dielectric layer 36 in Park. According to col. 2, lines 1-3 in Huang, "The etched back SOG 16 leaves rounded dips 24 in the surface between the tightly spaced metal lines and partially fills the broader regions 26." Furthermore, FIGS. 1 - 4 in Huang show the etched back SOG layer 16 to be thinner in the broader regions 26 than in the narrower regions between metal lines 14. Therefore, the prior art clearly demonstrates non-planarity in etched back dielectric layers that were

deposited over line patterns wherein the "dielectric layer is etched a certain distance below the top of the metal lines".

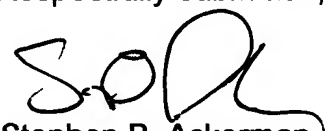
With respect to the Examiner's comments on page 9 that Huang teaches an etching back step that allows for +/- 5% uniformity. The Applicants submit that the Huang etch refers only to the dielectric layer and it is the dielectric layer thickness that has +/- 5% uniformity. The Applicants +/- 5 Angstrom variation in the cap layer is equivalent to substantially less than a +/- 5% variation since the cap layer thickness is referred to as "a few hundred Angstroms" in line 22 on page 13. Therefore, the improvement noted by the inventors is not anticipated by Huang.

The Applicants respectfully submit that none of the applied or known references address the claimed invention as described in claims 1 to 7, 8 to 21, and 23, 24 in which an insulation layer is first planarized by a CMP process that stops above a MTJ element and is then selectively etched back to a planarized surface at a certain level below the cap layer in the MTJ element. The claimed invention is believed to be patentable over the prior art cited, as it is respectfully suggested that the combination of the AAPA, Huang, and Park references does not teach an etch back of a previously planarized layer from a level above a MTJ to a certain level below the top surface of the MTJ. Applicant has claimed his process in detail. The processes of FIGS. 5 - 11 (claims 1 - 7, 9-21, 23, 24) are believed to be novel and patentable over the applied references. We therefore request Examiner Kennedy to reconsider her objection in view of the aforementioned arguments.

Since independent claims 1 and 11 are now believed to be patentable, the dependent claims 2 - 7, 9, 10, 12 - 21, and 23 - 24 are believed to be patentable. All claims are now believed to be in condition for allowance, and allowance is so requested.

It is requested that should there be any problems with this Amendment, please call the undersigned Attorney at (845) 452-5863.

Respectfully submitted,



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